Designing Testable Boards and Systems using Standard Design-For-Test (DFT) Techniques

Presented by Joseph E. Kadaras, DFT Consultant

DURATION: 2 days covering material from JEK-Tech™ Courses;

1/2 Day
A Historical view of Manufacturing Test
The Evolution of In-Circuit & Design-For-Test (DFT) Techniques
DFT solutions for real problems

1 Day
Overview Course on Board & System Level Boundary Scan
Design-For-Test (DFT) & Test Implementation.

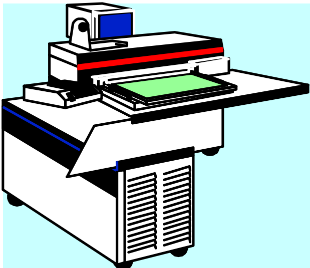
1/2 Day
Advanced Applications of formalized DFT.
1532 In System Configuration (ISC), IEEE 1149.6 Advanced
I/O test, Embedded Scan, System Test, SJTAG, P1581, P1687.

TARGET AUDIENCE: Digital board/system designers, field-service and test engineers, project managers, product support engineers.

MOTIVATION OBJECTIVES: To motivate chip and board designers to consider life-cycle test needs as an integral part of a product design process to the point where they proactively design in testability.

TEACHING OBJECTIVES: To identify the life-cycle needs of a product in respect of test. To present the basics Board and System level electrical test and identify the need for Design-For-Test (DFT) techniques that improve product quality and test process deployment, through re-use of DFT techniques. Identify areas of improvement through Concurrent Engineering of DFT Techniques.

Day 1 – First ½ day
An introduction to In-Circuit Test (ICT), In-Circuit Design-For-Test (DFT) & Beyond

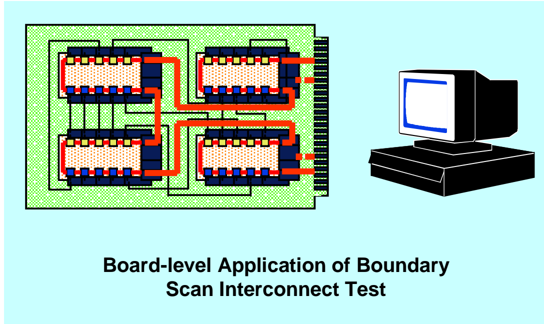


This seminar is ½ Day and is an introduction to the widely used technique of In-Circuit Board Testing. This tutorial covers an overview of In-Circuit test, from basic In-Circuit fixturing and test techniques to more advanced dual-level fixturing for secondary POST/BIST test. This tutorial defines a baseline for Design-For-Test techniques that can optimize ICT deployment and provides a foundation of understanding for the next generation of formalized Design-For-Test techniques.

In-Circuit test: What is it, how it works, and how to optimize test capabilities with DFT Techniques.

- Motivation for In-Circuit Test: Process improvement, cost effective fault isolation and diagnosis.
- In-Circuit Test Fixturing: Nodal Access and associated issues.
- In-Circuit Electrical Test Techniques: Testing Analog, Digital, Cluster, POST/BIST circuits.
- In-Circuit Design-For-Test: The good, the bad and the ugly (not necessarily in that order).
- In-Circuit Test: Evolution or End-of-Life?

Day 1 – Second ½ day & Day 2 – First ½ day
An introduction to the 1149.1 Boundary Scan Standard and supportive Design-For-Test Techniques



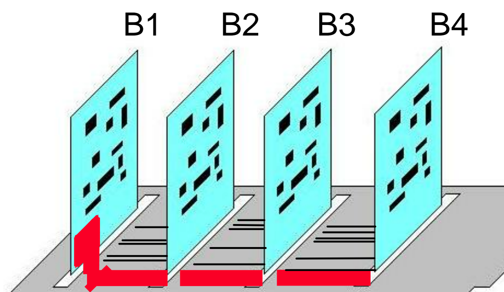
Board-level Application of Boundary Scan Interconnect Test

This seminar is a full day introduction to the widely-accepted IEEE 1149.1-2001 Boundary Scan Standard and shows how boundary scan can be used to ease the prototype debug and volume manufacturing test of loaded printed-circuit board assemblies. The seminar covers the basic chip-level architecture and Boundary-Scan Description Language (BSDL). The emphasis will be on the use of 1149.1 and benefits at board level. Pattern generation for detection and diagnosis of faults within the boundary scan domain will be discussed. Handling faults outside the domain (cluster and memory-array tests) are also considered.

THE IEEE 1149.1-2001 TEST ACCESS PORT AND BOUNDARY-SCAN ARCHITECTURE STANDARD

- Motivation for boundary scan: use of surface mount packaging, double-sided multi-layer boards
- Device-level architecture: Test Access Port (TAP), Instruction Register, TAP controller, Bypass register, Identification register, Boundary-Scan register, access to internal registers
- Mandatory and optional public instructions: BYPASS, EXTEST, PRELOAD, SAMPLE, INTEST, IDCODE, USERCODE, CLAMP, HIGHZ, RUNBIST
- Conducting a "blind" interrogation
- Forms of boundary-scan cells: BC_1 to BC_10
- Using boundary scan at board level: board defects and fault models (opens and shorts: equivalent fault models)
- Scan path integrity test
- Interconnect test: generating patterns to detect and locate interconnect opens and shorts
- Languages and formats: Boundary Scan Description Language (BSDL)
- Handling the BS-to-nonBS interface: creating tests for RAM and non-RAM clusters
- Practical chip and board DFT guidelines
- Advanced DFT Techniques: Optimizing board level Boundary Scan test coverage

Day 2 – Second ½ day
Advanced Applications of formalized DFT: In-System Configuration, System Test, Field-Service Test…



IEEE 1149.1 boundary scan was originally intended to solve board test interconnect problems on limited access boards. Boundary-scan technology now has a much-wider application to all manner of board and system test problems (some refer to it as "The Internet of Test"). Several companies supply boundary-scan support devices that allow 1149.1 to be used as a backplane test bus, opening up backplane interconnect test and multi-drop architectures, enabling backplane-to-board-to-chip diagnostics, in-system integration and field service scenarios. This tutorial covers these and other advanced applications of Boundary Scan, formalizing DFT across the test process.

This tutorial provides insight into advanced DFT applications and other IEEE Standards that maximize the use of on-board boundary-scan devices.

IEEE 1532-2002 IN-SYSTEM CONFIGURATION STANDARD

- Extensions to BSDL: flows, procedures and actions

IEEE 1149.4-1999 MIXED-SIGNAL TEST BUS STANDARD (OPTIONAL)

- Architecture, Test Bus Interface Circuit, internal test buses

IEEE 1149.6 & TESTING HIGH-SPEED BUSES

- Parallel/serial high-speed buses
- PCI-Express and other high-speed buses
- SerDes design styles
- Need for at-speed test
- Loopback test styles:
    - All in the chip (e.g. Intel® I-BIST)
    - All in the ATE channel card
    - Hybrid solution
- IEEE 1149.6-2003 "AC-EXTEST" Standard
- IEEE 1149.6 & changes to BSDL
- Modified TX boundary-scan cell
- Modified RX test receiver
- AC-PULSE and AC-TRAIN instructions
- Combinations of DC and AC coupling

USING 1149.1 AS A SYSTEM-LEVEL BACKPLANE TEST BUS FOR MULTI-BOARD SYSTEMS

- Using 1149.1 as a backplane bus: ring, star and multi-drop architectures
- The need for special enabling devices: backplane test-bus-master controllers, addressable gateway devices, and test-program sequencers
- Principles of backplane board-to-board interconnect test

STATUS OF THE SJTAG, P1581, P1687 and 1149.7, Emulation test and INEMI INITIATIVES

- What are they?
- What problems are being solved?

PUTTING IT ALL TOGETHER

- Leveraging DFT techniques "above the chip" and "above the board": product life-cycle view

SOURCES OF FURTHER INFORMATION

Attendees will receive a copy of the presentation slides.

COURSE PRESENTER: **Joseph E. Kadaras**

Joe has over 30 years of hands-on test experience ranging from Known-Good-Die & MCM test, to board/assembly level test, to system integration and test. Joe has been deploying IEEE1149.1 for 20+ years, acquiring first hand DFT test implementation experience. Joe started his career with the USAF, was a Principal Test Software Engineer with Digital Equipment Corporation, Test Engineering Manager with Mercury Computer Systems Inc. and was the Founder and Director of ASSET InterTech's Ensure Design-For-Test (EDFT) Services. In 2004 Joe founded JEK-Tech™, a Boundary Scan Test Solution provider and is now sharing his DFT knowledge worldwide.

Joe is a member of the Institute of Electrical and Electronic Engineers (IEEE), the IEEE P1581 working group, the American Society of Test Engineers (ASTE) and has several National and International Conference publications. Joe holds a Bachelors of Science degree from Franklin Pierce University.

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Baseline Course material provided in cooperation with Dr. R. G. "Ben" Bennetts, retired DFT Consultant.